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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/114,504	07/13/1998	ELIYAHOU HARARI		9326
36257	7590	10/25/2005		
PARSONS HSUE & DE RUNTZ LLP 595 MARKET STREET SUITE 1900 SAN FRANCISCO, CA 94105			EXAMINER	LE, VU ANH
			ART UNIT	PAPER NUMBER
			2824	

DATE MAILED: 10/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/114,504	HARARI ET AL. <i>[Signature]</i>	
	Examiner	Art Unit	
	Vu A. Le	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 07 March 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 63-65 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 63-65 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date: _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 63-65 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 63-65 recite **a data control logic circuit** for controlling a transfer of data between the outside of said flash memory card and the plurality of flash memory partitions through said connector and respectively transmitting block erase commands to the flash memory partitions including the physical blocks to be erased when the block erase commands associated with a plurality of blocks are inputted via said connector; and **an address control logic circuit** for managing addresses for the plurality of blocks inputted via said connector so as to disperse into the plurality of flash memory partitions by assigning the addresses to their corresponding addresses for the physical blocks of the plurality of flash memory partitions and for respectively transmitting chip enable signals to at least two of the plurality of flash memory partitions including the physical blocks to be erased in such a manner that when the block erase commands are inputted via said connector, a period in which said at least two flash memory partitions

are simultaneously busy, exists. The data control logic circuit and the address control logic circuit are two separate circuits while the specification shows only one controller 31 (Fig.1) for controlling flash EEPROM array 33. The controller 31 can not be considered as a **data control logic circuit** since the controller 31 does not **"transmitting block erase commands** to the flash memory partitions including the physical blocks **to be erased** when the block erase commands associated with a plurality of blocks are inputted via said connector". The specification teaches "the controller then issues to the circuit 220, as well as all other chips in the system a global erase command in line 251 along with the high voltage for erasing in line 209" (page 10, lines 33-35 and page 11, line1). It means that the controller of the present invention **issues a global** erase command (not **transmitting a block** erase command) to all other chips in the system (not to only the flash memory partitions including the physical blocks to be erased, the data control logic block does not transmitting block erase commands to the flash memory partitions which do not have the physical blocks to be erased). The controller 31 can not be considered as "an address control logic circuit for managing addresses ...by **assigning the addresses to their corresponding addresses for the physical blocks of the plurality of flash memory partitions**" since the controller 31 does not managing addresses for plurality of blocks by assigning the addresses to their corresponding addresses to the physical blocks". The specification only teaches "**the controller sends the address of the sector 211 to the circuit 220**" (page 10, lines 13-14). Furthermore, the controller 31 can not be considered as the address control logic circuit

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since the controller 31 does not "transmitting chip enable signals to at least two of the plurality of flash memory partitions including the physical blocks to be erased".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vu A. Le whose telephone number is (571) 272-1871. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Vu A. Le
Primary Examiner
Art Unit 2824

10/21/05